MIPS32 4K™ LV (4Kc, CSM J25C1) Specification Update

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Preface

This document communicates updates to the specifications of the family of MIPS32 4K™ and MIPS64 5K™ Processor Lead Vehicles contained in the document *MIPS 4K/5K™ Lead Vehicle Datasheet*, Ref[1].

There are variations in the characteristics of the Lead Vehicles. These are due to the variations in the type, revision, and configuration of the Lead Vehicle, and they are dependent on the vendor, the process technology, and the production series. Through the on-going validation and characterization of the Lead Vehicles, MIPS identifies updates and additions to the information in the documentation for the Lead Vehicles. The Specification Updates in this document are specific to the

- *MIPS32 4K Processor Lead Vehicle with manufacturing ID CSM J25C1*.

The Specification Updates can be classified as deviations from the generic specifications, additional information, or defects.

The document is primarily intended for hardware system developers building boards equipped with MIPS32 4K or MIPS64 5K Processor Lead Vehicles.

The document presents additional information and detailed descriptions of defects and deviations from the specifications in the Datasheet. There are sections for updates to the chip pin description, AC & DC specifications, power supply, operating frequency, and other specification updates.

When the Update is a defect, the sections include descriptions of the problem, the implications on the system, a suggested workaround, and a status. The status of a defect will be described by one of the following codes:

Table 1 Status Codes used in Summary Tables

Code	Description
Open	This issue is under investigation.
Fix	This issue is intended to be fixed in a future version of the component.
Fixed	This issue has been fixed in a previous version.
NoFix	There are no plans to fix this issue.
Doc	The appropriate documents will be updated in the future.

Emphasis of Range Violations and Document Modifications

Throughout the document a shaded field in a table is used to emphasize that this value is deviating from, or violating, the range specified in the Datasheet.

1 Specification Updates to CSM 0.25um LV

In the following, additional specific information on this particular Lead Vehicle is provided. The information is structured as a set of sub-sections containing specifications that must be present for each Lead Vehicle. These sub-sections are a supplements to the Datasheet and consist of:

- Basic Information
- Supply Voltages
- Test-related Pin-out
- DC Specifications
- AC Specifications
- PLL Connections and Loop Filter

These are followed by a sub-section on Specification Updates that are unique for this Lead Vehicle and are not covered elsewhere. The Updates do have a tracking number prefixed with the letter U (for Update). The following table lists the Updates and their status.

Table 2 Summary of Specification Updates

Update Number	Description	Status
U1	PLL is not functional in CSM J25C1 silicon, so operation in SYSAD64 mode is not possible. Only core bond-out mode can be used.	NoFix

1.1 Basic Information

The basic information for the Lead Vehicle is summarized in the following table.

Throughout this document, the newest pin naming style convention has been followed. That is the style where all low-active pins end in “_n” and where the old style suffix “p” has been dropped from all high-active pins.

Table 3 Lead Vehicle Information

Vendor	Chartered Semiconductor Manufacturing, Inc.
Type	MIPS32 4Kc™ core
Part ID	CSM J25C1
Data Cache	4-way, 4 kByte sets, 16 kByte total
Instruction Cache	4-way, 4 kByte sets, 16 kByte total
MMU	TLB with 16 dual entries
EJTAG Support	4 I breaks, 2 D breaks, TAP module
RTL Version	2.0

Table 3 Lead Vehicle Information (Continued)

Static Input Signals to Core: EJ_ManufID[10:0] EJ_PartNumber[15:0] EJ_Version[3:0]	 0 0 0
CP0 PRID Value	0x018001

1.2 Supply Voltages

The Lead Vehicle's three power supply voltages, the I/O power supply, the core power supply, and the PLL power supply (quiet Vss, Vdd) are listed in the following table.

Table 4 Supply Voltages

VDD (I/O buffers)	CVDD (Core)	VDDA (PLL supply)
3.3V +/-10%	2.5V +/-10%	2.5V +/-10%

When powering on the power supplies, it is recommended to first power up the I/O VDD supply, followed by the CVDD and VDDA supplies. The recommended power-down order of the supplies is the reverse of the power-up order; first power down the CVDD and VDDA supplies, then power down the I/O VDD supply.

1.3 Test-Related Pin-Out

The following table lists deviations and additions to the functional pin descriptions given in the Datasheet. Table 5 shows the format of the implementor test pins. The test pins are only for internal undocumented use. During normal operation, the test input pins should be left de-asserted, as shown in the "Disable Value" column of the table.

Table 5 Test Pin Descriptions

Test mode pins (implementor use only)				
Pin name	**Type**	**Control Pin**	**Disable Value for Normal Mode**	**Description**
TIN[0]	I		0	Non-public. For production test. Memory BIST test mode enable.
TIN[1]	I		0	Non-public. For production test. Memory BIST reset.
TIN[2]	I		0	PLL powerdown. When asserted, disables PLL and places it in low power state.
TIN[3]	I		0	External PLL divider selection pin: 0: Select external divide-by-4. 1: Select external divide-by-2.
TOUT[0]	O		N/A	Non-public. For production test. Instruction Cache BIST complete indication.

Table 5 Test Pin Descriptions (Continued)

TOUT[1]	O		N/A	Non-public. For production test. Instruction Cache BIST failure indication.
TOUT[2]	O		N/A	Non-public. For production test. Data Cache BIST complete indication.
TOUT[3]	O		N/A	Non-public. For production test. Data Cache BIST failure indication.
PLL_TRI	I		1	Tristate control pin for PLL_OUT output. If high, then the PLL_OUT pin is tristated.
PLL_OUT	O	PLL_TRI	N/A (tristate)	PLL output: VCO frequency output at multiplied frequency. Tristated when PLL_TRI is high.
PLL_LOCK	O		N/A	PLL lock indication.

1.4 DC Specifications

There are several types of input-only, output-only, and input/output buffers used in this Lead Vehicle. DC operating conditions are described in Table 6. Input and output voltage levels are shown in Table 7.

Table 6 Recommended Operating Conditions

Parameter	Description	Min	Nom	Max
VDD	I/O buffer supply voltage	3.0 V	3.3 V	3.6 V
V_I	Input voltage	0 V		VDD
V_O	Output voltage	0 V		VDD
V_{IH}	High-level input voltage	2.0 V		VDD + 0.3 V
V_{IL}	Low-level input voltage	-0.3 V		0.3 VDD

Table 7 Electrical Characteristics

Parameter	Condition	Min	Max
V_{OH}	I_O = - 1 ma, VDD = Min	2.4 V	
V_{OL}	I_O = 1 ma, VDD = Min		0.4 V
I_{IH}	$V_I = V_I$ Max, VDD = Max		+/- 15 µA
I_{IL}	$V_I = V_I$ Min, VDD = Max		+/- 15 µA

The input receivers all use the same CMOS input-only, non-inverting pads, IN1. The output pads are all 3.3v TTL outputs. Several types of outputs pads are used, as described in Table 8. For the output drivers the rated AC drive current, I_O, is included in the table as well.

Table 8 Driver Characteristics

Driver	Description	I/O	I_O
IN1	CMOS input-only pad	I	N/A
OUT4	TTL output-only pad	O	4 mA

Table 8 Driver Characteristics (Continued)

Driver	Description	I/O	I_O
OUT8	TTL output-only pad	O	8 mA
OUTTR4	TTL tristate output-only pad with pulldown resistor	O	4 mA
OUTT8	TTL tristate output-only pad	O	8 mA
INOUT8	TTL input/output pad	I/O	8 mA

1.5 AC Specifications

This section shows any deviations of the AC specifications from the corresponding descriptions in the Datasheet. All violations of the previous described value ranges are highlighted with a shaded background in the table. First, an overview of the clock AC specifications is provided. Then, tables for the AC requirements of the pins are presented.

1.5.1 Clock Signals

The table below (Table 9) shows the frequency and duty cycle ranges for all the input clock pins in the Lead Vehicle. The duty cycle is here specified as the percentage of the cycle where the phase is high.

Since the PLL is not functional is this Lead Vehicle, operation in SYSAD64 mode is not possible. Only clocking related to core bond-out mode is described.

Table 9 Clocking Frequency and Duty Cycle Range

Pin, Mode	Min	Max
Core clock frequency range.	0 MHz	76 MHz
GCLK frequency range, core bond-out (PLL disabled)	0 MHz	75 MHz
GCLK duty cycle, core bond-out (PLL disabled)	40	60
ETCK frequency range	0 MHz	40 MHz
ETCK duty cycle	min. 10 ns high, and min. 10 ns low	

1.5.2 Other Functional Pins

The following tables list the AC/DC pin specifications. Values that violates the ranges specified in the Datasheet are highlighted using a shaded background.

Note that the AC/DC table for SYSAD64 mode is not shown here since the PLL required for SYSAD64 mode is not functional in this Lead Vehicle and this mode cannot be used.

Table 10 AC/DC Pin Specs for Shared Function Pins

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
GCLK	I	IN1						
GCLKB	O	OUT8	25	GCLK				
GRST2_N	I	IN1		DC				
GBYPASS	I	IN1		DC				
GMULT[1:0]	I	IN1		DC				
CBIGEN	I	IN1		DC				
CTIMER5	I	IN1		DC				
CSYSAD	I	IN1		DC				
CPIPEWR	I	IN1		DC				
C4WBLK	I	IN1		DC				
ETCK	I	IN1						
ETMS	I	IN1		DC				
ETDI	I	IN1		ETCK			4	1
ETDO	O (3S)	OUTT8	25	ETCK[a]	2	5.4		
ETRST_N	I	IN1		DC				
EDINT	I	IN1		ASYNC				
ERES[11:0]	O	OUT8	50					
TSE	I	IN1		DC				
TSM	I	IN1		DC				
TSI	I	IN1		DC				
TSO	O	OUT8	25					
TIN[3:0]	I	IN1		DC				
TIN_N[3:0]	I	IN1		DC				
TOUT[3:0]	O	OUT8	25					
MBUS	I	IN1		DC				
MINP[3:0]	I	IN1		DC				
MINP_N[3:0]	I	IN1		DC				

a. The ETDO output timing is specified relative to the negative edge of ETCK.

Table 11 AC/DC Pin Specs for Core Bond-out Mode

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
EB_A[35:2]	O	OUT8	25	GCLK	3	11.1		
EB_WData[63:0]	O	OUT8	25	GCLK	3	10.7		
EB_RData[63:0]	I	IN1		GCLK			6	0
EB_BE[7:0]	O	OUT8	25	GCLK	3	10		
EB_AValid	O	OUT8	25	GCLK	3	10.3		
EB_Write	O	OUT8	25	GCLK	3	10		
EB_Instr	O	OUT8	25	GCLK	3	10		
EB_Burst	O	OUT8	25	GCLK	3	10.1		
EB_BFirst	O	OUT8	25	GCLK	3	10		
EB_BLast	O	OUT8	25	GCLK	3	10		
EB_BLen[1:0]	O	OUT8	25	GCLK	3	10		
EB_ARdy	I	IN1		GCLK			6	0
EB_RdVal	I	IN1		GCLK			6	0
EB_WDRdy	I	IN1		GCLK			6	0
EB_RBErr	I	IN1		GCLK			6	0
EB_WBErr	I	IN1		GCLK			6	0
EB_WWBE	O	OUT8	25	GCLK	3	10		
EB_EWBE	I	IN1		GCLK			6	0
EB_SBlock	I	IN1		GCLK			6	0
SI_Int[5:0]	I	IN1		GCLK			6	0
SI_NMI	I	IN1		GCLK			6	0
SI_ColdReset	I	IN1		GCLK			6	0
SI_Reset	I	IN1		GCLK			6	0
SI_MergeMode[1:0]	I	IN1		GCLK			6	0
SI_RP	O	OUT8	25	GCLK	3	10		
SI_Sleep	O	OUT8	25	GCLK	3	10		
SI_TimerInt	O	OUT8	25	GCLK	3	10		
SI_ERL	O	OUT8	25	GCLK	3	10		
SI_EXL	O	OUT8	25	GCLK	3	10		

Table 11 AC/DC Pin Specs for Core Bond-out Mode (Continued)

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
EJ_PerRst	O	OUT8	25	GCLK	3	10		
EJ_PrRst	O	OUT8	25	GCLK	3	10		
EJ_SRstE	O	OUT8	25	GCLK	3	10		
EJ_DebugM[a]	O	OUT8	25	GCLK	N/A	N/A		
PM_DCacheHit	O	OUT8	25	GCLK	3	10		
PM_DCacheMiss	O	OUT8	25	GCLK	3	10		
PM_ICacheHit	O	OUT8	25	GCLK	3	10		
PM_ICacheMiss	O	OUT8	25	GCLK	3	10		
PM_InstnComplete	O	OUT8	25	GCLK	3	10		
PM_ITLBHit	O	OUT8	25	GCLK	3	10		
PM_ITLBMiss	O	OUT8	25	GCLK	3	10		
PM_JTLBHit	O	OUT8	25	GCLK	3	10		
PM_JTLBMiss	O	OUT8	25	GCLK	3	10		
PM_WTBMerge	O	OUT8	25	GCLK	3	10		
PM_WTBNoMerge	O	OUT8	25	GCLK	3	10		
PM_DTLBHit[b]	O	OUT8	25	GCLK	N/A	N/A		
PM_DTLBMiss[b]	O	OUT8	25	GCLK	N/A	N/A		

a. The EJ_DebugM signal isn't driven on this LV.

b. The PM_DTLBHit and PM_DTLBMiss pins are not driven on this device, as it does not contain a DTLB. The value on those pins is therefore undefined.

1.6 PLL Connections and Loop Filter

The following table shows the pin-out for the 6 analog connections to the PLL (quiet supplies, optional loop filter etc.). The PLL in this Lead Vehicle design does not have an external loop filter, so the LF pin (C14) should be left unconnected. The specific connections are described below.

Table 12 PLL Pin-out

B13	D13	A13	C14	B12	C13
PLL_TRI (PLL_NC[2])	PLL_OUT (PLL_NC[1])	VSSA	NC	VDDA	PLL_LOCK (PLL_NC[0])

2 Software-configurable Features of the 4K Core in the Lead Vehicle

This Lead Vehicle allows the manipulation of some otherwise read-only bits in the CP0 Config register. The features that can be modified are the MMU type field in the Config Select 0 Register, and the cache configuration bits in the Config Select 1 Register. The ability to change these features in software enables evaluation and benchmarking of the fixed memory management unit present in other members of the 4K processor core family, as well as the effect of different caches sizes and organizations beyond the default cache implemented on this Lead Vehicle.

The features described in this section are present specifically to support configuration testing of the core in a Lead Vehicle, and are not supported in any other environment. Attempting to use these features outside of the scope of a Lead Vehicle is a violation of the MIPS Architecture, and may cause unpredictable operation of the processor.

2.1 Config Register Format — Select 0

31	30		28	27		25	24			21	20	19	18	17	16	15	14	13	12		10	9		7	6			3	2		0
M	K23			KU			R				MDU	WC	MM		BM	BE	AT		AR			MT			0				K0		

The format of Config (Select 0) Register is shown above and the bit fields are described in Table 13. Most of the fields are identical to the description of this register in the *MIPS32 4K™ Processor Core Family Software User's Manual*, but the whole register is shown here for completeness. The modified fields relevant to the software configuration features are highlighted in bold type in the tables. Here is an overview of the modified fields in this register:

- WC (bit 19): This new read/write bit is a write enable for the software-configurable features within the Config Register available on this Lead Vehicle. It can be written to either 1 or 0, but is initialized to 0. When this field is set to 1, the MT field in Config Select 0 and the cache configuration fields in Config Select 1 become writeable.
- MT (bits 9:7): The MMU Type field, which is normally read-only, becomes writeable when WC is set. Since the only legal values of MT for the 4K cores are 0x1, indicating that a Translation Lookaside Buffer (TLB) -based memory management unit is present, or 0x3, indicating that a fixed Block Address Translation (BAT) -based MMU is present, only bit 8 within this field is actually writeable. Due to the implementation, the WC field must have been previously set to a 1 by an earlier MTC0 instruction before the MT field can be modified. So trying to set the WC bit (if it was previously cleared) and modify the MT field with the same MTC0 instruction will not modify the MT field.
- K23 (bits 30:28) and KU (bits 27:25): These fields control the cacheability of the kseg2/3 and kuseg/useg address segments. They are reserved fields (read as zero, writes are ignored) when the MT field is 0x1, indicating that a TLB is present. These fields become readable and writeable when the MT field is 0x3, indicating that a fixed BAT is present. Due to the implementation, the MT field must have been set to 0x3 by an earlier MTC0 instruction before the K23 and KU fields become writeable.

Table 13 Config Register Field Descriptions

Fields		Description	Read/ Write	Reset State
Name	Bit(s)			
M	31	This bit is hardwired to '1' to indicate the presence of the Config register.	R	Preset
K23	30:28	This field controls the cacheability of the kseg2 and kseg3 address segments in BAT implementations. This field is valid in the 4Kp and 4Km processor and is reserved in the 4Kc processor. Refer to Table 14 for the field encoding.		
KU	27:25	This field controls the cacheability of the kuseg and useg address segments in BAT implementations. This field is valid in the 4Kp and 4Km processor and is reserved in the 4Kc processor. Refer to Table 14 for the field encoding.		

Table 13 Config Register Field Descriptions (Continued)

Fields		Description	Read/ Write	Reset State
Name	Bit(s)			
R	24:21	Reserved. Returns a zero value when read.	R	0
MDU	20	This bit indicates the MDU type. 0 = Fast Multiplier Array (4Kc and 4Km) 1 = Iterative multiplier (4Kp)		
WC	**19**	**Write enable bit for MT field in Config Select 0 and cache configuration bits in Config Select 1.**	**R/W**	**0**
MM	18:17	This field contains the merge mode for the 32-byte collapsing write buffer: 00 = No Merging 01 = SysAD Valid merging 10 = Full merging 11 = Reserved	R	Preset
BM	16	Burst order. This bit is always zero to indicate sequential burst mode.	R	0
BE	15	Indicates the endian mode in which the processor is running: 0: Little endian 1: Big endian	R	Preset or Externally Set
AT	14:13	Architecture type implemented by the processor. This field is always 00 to indicate MIPS32.	R	Preset
AR	12:10	Architecture revision level. This field is always 000 to indicate revision 1. 0: Revision 1 1-7: Reserved	R	Preset
MT	**9:7**	**MMU Type:** **1: Standard TLB (4Kc)** **3: Fixed Mapping (4Kp, 4Km)** **0, 2, 4-7: Reserved**	**R/W**	**Preset**
0	6:3	Must be written as zero; returns zero on read.	0	0
K0	2:0	Kseg0 coherency algorithm. Refer to Table 14 for the field encoding.	R/W	Undefined

Table 14 Cache Coherency Attributes

C(2:0) Value	Cache Coherency Attribute
0, 1, 3*, 4, 5, 6	Cacheable, noncoherent, write-through, no write allocate
2*, 7	Uncached

Note: * These two values are required by the MIPS32 architecture. In the 4Kc and 4Kp processor cores, all other values are not used. For example, values 0, 1, 4, 5 and 6 are not used and are mapped to 3. The value 7 is not used and is mapped to 2.

Note: Note that these values do have meaning in other MIPS Technologies processor implementations. Refer to the MIPS32 specification for more information.

2.2 Config1 Register Format — Select 1

31	30					25	24		22	21		19	18		16	15		13	12		10	9		7	6	5	4	3	2	1	0
0	MMU Size						IS			IL			IA			DS			DL			DA			0			PC	WR	CA	EP	FP

The format of Config (Select 1) Register is shown above, and the bit fields are described in Table 15. Most of the fields are identical to the description of this register in the *MIPS32 4K™ Processor Core Family Software User's Manual* but the whole register is shown here for completeness. The modified fields relevant to the software configuration features are highlighted in bold type in the tables. Here is an overview of the modified fields in this register:

- The instruction cache configuration fields (IS, IL and IA) and the data cache configuration fields (DS, DL and DA) which are otherwise read-only become writeable when the WC bit in the Config Select 0 register is set. Note that only certain values for these fields are legal, while other encodings are reserved.

Table 15 Config1 Register Field Descriptions — Select 1

Fields		Description	Read/Write	Reset State
Name	Bit(s)			
0	31	This bit is reserved to and must be read or written as zero.	R	Preset
MMU Size	30:25	This field contains the number of entries in the TLB minus one. The field is read as 15 decimal in the 4Kc processor and as 0 decimal in the 4Kp and 4Km processors.	R	Preset
IS	**24:22**	**This field contains the number of instruction cache sets per way. Three options are available in both cores. All others values are reserved:** **0x0: 64** **0x1: 128** **0x2: 256** **0x3 - 0x7: Reserved**	**R/W**	**Preset**
IL	**21:19**	**This field contains the instruction cache line size. If an instruction cache is present, it must contain a fixed line size of 16 bytes.** **0x0: No Icache present** **0x3: 16 bytes** **0x1, 0x2, 0x4 - 0x7: Reserved**	**R/W**	**Preset**
IA	**18:16**	**This field contains the level of instruction cache associativity.** **0x0: Direct mapped** **0x1: 2-way** **0x2: 3-way** **0x3: 4-way** **0x4 - 0x7: Reserved**	**R/W**	**Preset**
DS	**15:13**	**This field contains the number of data cache sets per way:** **0x0: 64** **0x1: 128** **0x2: 256** **0x3 - 0x7: Reserved**	**R/W**	**Preset**
DL	**12:10**	**This field contains the data cache line size. If a data cache is present, it must contain a line size of 16 bytes.** **0x0: No Dcache present** **0x3: 16 bytes** **0x1, 0x2, 0x4 - 0x7: Reserved**	**R/W**	**Preset**

Table 15 Config1 Register Field Descriptions — Select 1 (Continued)

Fields		Description	Read/Write	Reset State
Name	**Bit(s)**			
DA	**9:7**	**This field contains the type of set associativity for the data cache:** **0x0: Direct mapped** **0x1: 2-way** **0x2: 3-way** **0x3: 4-way** **0x4 - 0x7: Reserved**	**R/W**	**Preset**
0	6:5	Must be written as zero; returns zero on read.	0	0
PC	4	Performance Counter registers implemented. Always a 0 since the cores do not implement any.	R	0
WR	3	Watch registers implemented. This bit is always read as 1 since the cores each contain one pair of Watch registers.	R	1
CA	2	Code compression (MIPS16) implemented. This bit is always read as 0 because MIPS16 is not supported.	R	0
EP	1	EJTAG present: This bit is always set to indicate that the core implements EJTAG.	R	1
FP	0	FPU implemented. This bit is always zero since the core does not contain a floating point unit.	R	0

2.3 MT Configuration in Config Select 0

The MT field in the Config Select 0 Register can be written, so that the default TLB-based memory management unit of 4Kc core within the Lead Vehicle can be configured to mimic the fixed Block Address Translation (BAT) memory management algorithm of the MIPS32 4Km™ and 4Kp™ cores.

Here is the sequence which must be used to accomplish a change in the MT field. This sequence should be executed in unmapped space to avoid unpredictable behavior.

1. MTC0 instruction to set WC field in Config Select 0.
2. An additional MTC0 instruction to write the MT field to its desired value.
3. If changing the MT field to select the fixed BAT-style MMU, then one or more additional MTC0 instructions are required to write the KU and K23 fields to desired values to control the cacheability of those regions. The KU and K23 fields can only be written when the MT value is 0x3.

2.4 Cache Configuration in Config Select 1

The cache configuration bits in the Config Select 1 Register can be written to modify the default cache size and organization.

Here is the sequence which must be used to accomplish a change in the cache configuration bits. This sequence should be executed in uncacheable space to avoid unpredictable behavior.

1. MTC0 instruction to set WC field in Config Select 0.
2. One or more additional MTC0 instructions to write the instruction and data cache configuration bits in Config Select 1 to their desired values.

Here are some additional considerations to keep in mind:

- Obviously, you cannot select a larger cache size or organization than the largest size present on the 4K core in the Lead Vehicle.
- The instruction and data caches can be configured independently.
- It is possible to disable a cache by setting the line size field (IL or DL) to zero.
- Only certain values for the cache configuration fields are legal in the 4K processor core, as detailed in Table 15.
- If you downsize or disable a cache with this method, only new line allocations are disabled. Loads or stores to “old” entries will still hit, even if they are in that part of the cache which has been downsized. If you do not desire this behavior, then you should initialize all the tag entries for the maximum cache configuration to be invalid before you select your new cache configuration.

Appendices

A References

[1] MIPS 4K/5K™ Lead Vehicle Datasheet
Document no: MD00001
MIPS Technologies, Inc.

B Revision History

Table 2-1

Revision	Date	Description
00.90	Feb. 4, 2000	Initial version for review.
00.91	Mar. 10, 2000	Updates based on review: • Included core type (4Kc) in document title. • Added comments about power-up/-down order for the supplies. • Removed tristate current entry from Table 7. • Removed load factor column from Table 8. • Renamed I/O buffers to use more generic descriptions. • Modified disclaimer about use of software-configurable features.
00.92	May 25, 2000	• Added Specification Update U1, noting that PLL is not functional, so SYSAD64 mode is not usable. Removed AC/DC table specific to SYSAD64 mode. • Updated ETDO pin timing in Table 10 to show that max clock-to-out timing does not meet Datasheet spec.
01.00	May 30, 2000	• Initial version for external release. • Updated copyright notice and document footer. • Converted note about PM_DTLB* signals to a footnote in Table 11. • Enhanced Table 5 to more clearly specify “off” value for test pin inputs.
01.01	May 31, 2000	• Added standard trademark notices.
01.02	Feb. 8, 2001	• Updated to new template format.